IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Vito Fabbrizio et al.

Application No. : 10/631,323

Filed : July 31, 2003

For : LOW-VOLTAGE, VERY-LOW-POWER CONDUCTANCE MODE NEURON

Art Unit : 2122

Docket No. : 03-I-712 (850063.603RI)

Date : May 19, 2005

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents:

In accordance with 37 CFR 1.56 and 1.97 through 1.98, applicants wish to make known to the U.S. Patent and Trademark Office the references set forth on the attached Form PTO-1449. Copies of the cited U.S. patents and published patent applications are not required and accordingly have not been provided. Copies of all other cited references are enclosed. As to any reference supplied, applicants do not admit that it is "prior art" under 35 U.S.C. §§ 102 or 103, and specifically reserve the right to traverse or antedate any such reference, as by a showing under 37 C.F.R. § 1.131 or other method. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicants' duty to disclose all information they are aware of which is believed relevant to the examination of the above-identified application, applicants believe that their invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

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Applicants believe this Information Disclosure Statement has been timely filed, however, the Commissioner is authorized to charge any fee due by way of this Information Disclosure Statement to our Deposit Account No. 19-1090.

Respectfully submitted,

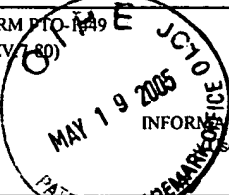Seed Intellectual Property Law Group PLLC

E. Russell Tarleton
Registration No. 31,800

Enclosures:
  Form PTO-1449
  Cited References (29)

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

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	INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Vito Fabbrizio et al.	
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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,956,564	09/11/90	Holler et al.	307	201	
	AB	4,961,002	10/02/90	Tam et al.	307	201	
	AC	4,988,891	01/29/91	Mashiko	307	201	
	AD	5,004,932	04/02/91	Nejime	307	201	
	AE	5,021,693	06/04/91	Shima	307	494	
	AF	5,021,988	06/04/91	Mashiko	364	807	
	AG	5,053,638	10/01/91	Furutani et al.	307	201	
	AH	5,056,037	10/08/91	Eberhardt	364	513	
	AI	5,101,361	03/31/92	Eberhardt	395	24	
	AJ	5,146,602	09/08/92	Holler et al.	395	23	
	AK	5,150,450	09/22/92	Swenson et al.	395	23	
	AL	5,155,377	10/13/92	Castro	307	201	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	NO
	AM	0 349 007 B1	12/20/95	EP		

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AN	Benson, R. et al., "UV-Activated Conductances Allow for Multiple Time Scale Learning," *IEEE Trans. on Neural Networks* 4(3):434-440, May 1993.
	AO	Boser, B. et al., "An Analog Neural Network Processor with Programmable Topology," *IEEE J. of Solid State Circuits* 26(12):2017-2025, December 1991.
	AP	Chandraksan, A. et al., "Low-Power CMOS Digital Design," *IEEE J. of Solid-State Circuits* 27(4):473-484, April 1992.
	AQ	Cosatto, E. et al., "NET31K High Speed Image understanding System," in *Proc. Fourth Intl. Conf. on Microelectronics for Neural Networks and Fuzzy Systems*, IEEE Computer Society Press, Los Alamitos, CA, 1994, pp. 413-421.

EXAMINER	DATE CONSIDERED

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	BA	5,155,802	10/13/92	Mueller et al.	395	24	
	BB	5,187,680	02/16/93	Engeler	364	807	
	BC	5,202,956	04/13/93	Mashiko	395	24	
	BD	5,248,956	09/28/93	Himes et al.	338	334	
	BE	5,256,911	10/26/93	Holler et al.	307	201	
	BF	5,258,657	11/02/93	Shibata et al.	307	201	
	BG	5,268,320	12/07/93	Holler et al.	437	43	
	BH	5,274,746	12/28/93	Mashiko	395	27	
	BI	5,298,796	03/29/94	Tawel	307	201	
	BJ	5,299,286	03/29/94	Imondi et al.	395	27	
	BK	5,305,250	04/19/94	Salam et al.	364	807	
	BL	5,336,937	08/09/94	Sridhar at el.	307	201	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION	
					YES	NO
	BM					

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	BN	Degrauwe, M. et al., "A Micropower CMOS-Instrumentation Amplifier," *IEEE J. of Solid-State Circuits* 20(3):805-807, June 1985.
	BO	Fabbrizio, V. et al., "Low Power, Low Voltage Conductance-Mode CMOS Analog Neuron," in *Proc. of MicroNeuro '96,* pp. 111-115, February 1996.
	BP	Graf, H. et al., "A CMOS Associative Memory chip," in *Proc. IEEE First Intl. Conf. neural Newtworks, M. Caudill and C. Butler (ed.),* SOS Printing, San Diego, CA 1987, pp. III-461 – III-468.
	BQ	Graf, H. et al., "A Reconfigurable CMOS Neural Network," *IEEE ISSCC,* pp. 144-145, February 1990.

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	CA	5,343,555	08/30/94	Yayla et al.	395	24	
	CB	5,396,581	03/07/95	Mashiko	395	24	
	CC	5,422,982	06/06/95	Pernisz	395	24	
	CD	5,444,821	08/22/95	Li et al.	395	24	
	CE	5,475,794	12/12/95	Mashiko	395	24	
	CF	5,509,105	04/16/96	Roenker et al.	395	24	
	CG	5,615,305	03/25/97	Nunally	395	24	
	CH	5,704,014	12/30/97	Marotta et al.	395	24	
	CI	6,032,040	02/29/00	Fabbrizio et al.	706	15	

FOREIGN PATENT DOCUMENTS

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					YES	NO
	CJ					

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	CK	Guardiani, C. et al., "Applying a Submicron Mismatch Model to Practical IC Design," in *Proc. of the CICC*, pp. 13.3.1-13.3.1, 1994.
	CL	Holler, M. et al., "An Electrically Trainable Artificial Neural Network (ETANN)with 10240 'Floating Gate' Synapses," in *Proc. IJCNN*, pp. 2.191-2.196, June 1989.
	CM	Hollis, P. et al., "Artificial Neural Networks Using MOS Analog Multipliers," *IEEE J. of Solid-State Circuits* 25(3):849-855, June 1990.
	CN	Jain, J. et al., "Displacement Measurement and Its Application in Interframe Image Coding," *IEEE Trans. on Communications COM-29*(12):1799-1808, December 1981.
	CO	König, A. et al., "Massively Parallel VLSI-Implementation of a Dedicated Neural Network for Anomaly Detection in Automated Visual Quality Control," in *Proc. of the 4th Intl. Conf of Microelectronics for Neural Networks and Fuzzy Systems*, Turin, Italy, September 26-28, 1994, pp. 354-364.
	CP	Kovács-V, Z. et al., "Massively-Parallel Handwritten Character Recognition Based on the Distance Transform," *Pattern Recognition 28*(3):293-301, 1995.

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	DB					

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	DC	Kramer, A. et al., "EEPROM Device as a Reconfigurable Analog Element For Neural Networks," *IEDM Tech. Digest*, pp. 10.3.1-10.3.4, December 1989.
	DD	Kramer, A. et al., "Ultra-Low-Power Analog Associative Memory Core Using Flash-EEPROM-Based Programmable Capacitors," in *Proc. of the 1995 Intl. Symposium on Low Power Design*, Assoc. for Computing Machinery, Dana Point, CA, 1995, pp. 203-208.
	DE	Kramer, A. et al., "Flash-Based Programmable Nonlinear Capacitor for Switched-Capacitor Implementations of Neural networks," *IEDM Tech. Dig.*, pp. 17.6.1-17.6.4, December 1994.
	DF	Lazzaro, J. et al., "Systems Technologies for Silicon Auditory Models," *IEEE Micro* *14*(3):7-15, June 1994.
	DG	Lee, B. et al., "Analog Floating-Gate Synapses for General-Purpose VLSI Neural Computation," *IEEE. Trans. on Circuits and Systems 38*(6):654-658, June 1991.
	DH	Mizugaki, Y .et al., "Implementation of New Superconducting Neural Circuits using Coupled SQUIDs," *IEEE Transcriptions on Applied Superconductivity 4*(1):1-8, March 1994.
	DI	Sage, J. et al., "An Artificial Neural Network Integrated Circuit Based on MNOS/CCD Principles," in *Proc. Conf. Neural Networks for Computing, J.S. Denker (ed.)*, Amer. Inst. of Physics, Snowbird, UT, 1986, pp. 381-385.
	DJ	Satyanarayana, S. et al., "A Reconfigurable VLSI Neural Network," *IEEE J. Solid-State Circuits 27*(1):67-81, January 1992.
	DK	Seevinck, E. et al., "A Versatile CMOS Linear Transconductor/Square-Law Function Circuit," *IEEE J. Solid-State Circuits SC-22*(3):366-377, June 1987.
	DL	Sin, C-K. et al., "EEPROM as an Analog Storage Device, with Particular Applications in Neural Networks," *IEEE Trans. on Electron Devices 39*(6):1410-1419, June 1992.

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	EF						
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	EH					
	EI					
	EJ					

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	EK	Sze, S., *Physics of Semiconductor Devices*, 2 ed., Wiley, 1981, p. 403.
	EL	Tomasini, S. et al., "B/W Adaptive Image Grabber with Analog Motion Vector Estimator at 0.3GOPS," *ISSCC Dig. of Tech. Papers*, pp. 94-95, 425, 1996.
	EM	Tsukano, K. et al., "A New CMOS Neuron Circuit based on a Cross-Coupled Current Comparator Structure," *IEICE Trans. on Fundamentals of Electronics, Comm. and Computer Sciences E75-A*(7):937-943, July 1992.
	EN	White, M. et al., "Electrically Modifiable Nonvolatile Synapses for Neural Networks," *IEEE Intl. Symposium on Circuits and Systems 2*:1213-1216, May 1989.

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